REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-7, 9-18, 20-32, and 34-41 remain pending. Claims 1-7, 9-18, 20-32, and 34-41 have been rejected.

Claims 1, 7, 12, 18, 23, 25, and 26 have been amended. Claims 5, 6, 8, 16, 17, 19, 30, 31, 33, and 34 have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38 and 40-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,282,556 to Chehrazi et al. ("Chehrazi") in view of U.S. Patent No. 6,036,350 to Mennemeier ("Mennemeier").

Amended claim 1 reads as follows:

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
>
> receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the register file;
>
> selecting a first plurality of numbers of the first vector from a string of bits in the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers; and
>
> generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers;
>
> wherein the third plurality of numbers are saved in a third entry in the register file;
>
> wherein the above operations are performed in response to the microprocessor receiving the single instruction, wherein the single instruction indicates the first entry for the first plurality of numbers, the second entry for the second plurality of numbers, and the third entry for the third plurality of numbers in the register file.

(emphasis added)

As set forth above, amended claim 1 requires selecting a first plurality of numbers of the first vector from a string of bits in the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers.

Chehrazi discloses the following:

> FIG. 20A and FIG. 20B illustrate the operation of the sum of absolute differences instruction called the SABD instruction. The SABD instruction of the present invention executes within two execution pipestages and the data is written back in the writeback pipestage. FIG. 20A illustrates an exemplary format 560 of the SABD instruction. The SABD operation computes the differences between corresponding operands stored in the operand registers, Vt and Vs, under control of the format field, determines the absolute value of these differences then adds the absolute value differences together to arrive at a final sum. The resultant sum value is stored in the least significant half word of the destination register, Vd. The operands can be signed or unsigned packed bytes as specified by the formal field 560e. The SABD instruction 560 specifies the source or input registers Vt and Vs by fields 560d and 560c, respectively, and specifies the destination register, Vd, in field 560b. Different modes of operation are possible of the SABD instruction and these are specified in the mode field 560e.

(Chehrazi, col. 20, lines 43-60)(emphasis added)

In particular, Chehrazi discloses the following:

> FIG. 20B is a diagram 570 that illustrates the operation of the SABD instruction in one exemplary mode. Input register 310 contains 16 separate 8-bit operands called 310(a)-310(p). Input register 312 contains 16 separate 8-bit operands called 312(a)-312(p). As shown in FIG. 20B, each separate operand of register 310 has a corresponding operand of register 312, e.g., operand 310(f) corresponds to operand 312(f), etc. The data path circuit 300 first uses one of its 16 8-bit subtractor circuits, 322 or 324 (FIG. 4), to perform subtraction on each corresponding operand pair, specifically subtracting Vs from Vt. The other 16 8-bit subtractor circuit then performs the same subtraction in parallel but between Vt from Vs. This simultaneously products 32 separate differences and a positive and a negative difference for each corresponding operand pair. Multiplexers in circuit 332 then select the positive difference for each operand pair as the absolute value difference for each pair. These absolute value differences are them summed together at 575 of FIG. 20B to arrive at a single result sum stored in register 415.

(Chehrazi, col. 20, line 61- col. 21, line 12) (emphasis added)

Thus, Chehrazi discloses that the SABD instruction specifies the input register consisting of 16 separate 8-bit operands. In contrast, amended claim 1 refers to the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers. Chehrazi fails to disclose, teach, or suggest selecting a first plurality of numbers of the first vector from a string of bits in the first entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers, as recited in amended claim 1.

Mennemeier, in contrast, discloses sorting signed numbers and solving absolute differences using packed instructions (Abstract). Mennemeier fails to disclose, teach, or suggest selecting a first plurality of numbers of the first vector from a string of bits in the first entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers, as recited in amended claim 1.

Thus, neither Chehrazi, nor Mennemeier, discloses such limitations of amended claim 1.

It is respectfully submitted that Chehrazi does not teach or suggest a combination with Mennemeier, and Mennemeier does not teach or suggest a combination with Chehrazi. Chehrazi addresses the pipelined data path architecture. Mennemeier, in contrast, addresses sorting the signed numbers. It would be impermissible hindsight, based on applicants' own disclosure, to combine Chehrazi and Mennemeier.

Furthermore, even if Chehrazi and Mennemeier were combined, such a combination would still lack selecting a first plurality of numbers of the first vector from a string of bits in the first entry according to a configuration specified by the instruction that indicates a way

how to partition the string of bits in the first entry into the first plurality of numbers, as recited in amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier.

For at least the reasons that are similar to those discussed above with respect to amended claim 1, applicants respectfully submit that claims 3, 7, 9-14, 18, 20-28, 32, 35-38 and 40-41 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier. Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chehrazi in view of Mennemeier as applied to claims 1, 2, 12, 26, and 27 above, and further in view of EP Application No. EPO 0485776 A2 to Diefendorff et al.

As set forth above, a combination of Chehrazi and Mennemeier fails to disclose selecting a first plurality of numbers of the first vector from a string of bits in the first entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers, as recited in amended claim 1.

Diefendorff, in contrast, discloses a method for executing graphics pixel packing instructions in a data processor.

Furthermore, even if Mennemeier, Diefendorff and Chehrazi were combined, such a combination would still lack selecting a first plurality of numbers of the first vector from a string of bits in the first entry according to a configuration specified by the instruction that indicates a way how to partition the string of bits in the first entry into the first plurality of numbers, as recited in amended claim 1.

Given that claims 4, 15, 29, and 39 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 4, 15, 29, and 39 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier, and further in view of Diefendorff.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 022666 for any fee deficiency that may be due.

Respectfully submitted,

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